Integrated logic circuits using single-atom transistors

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Scaling down the size of computing circuits is about to reach the limitations imposed by the discrete atomic structure of matter. Reducing the power requirements and thereby dissipation of integrated circuits is also essential. New paradigms are needed to sustain the rate of progress that society has become used to. Single-atom transistors, SATs, cascaded in a circuit are proposed as a promising route that is compatible with existing technology. We demonstrate the use of quantum degrees of freedom to perform logic operations in a complementary-metal–oxide–semiconductor device. Each SAT performs multilevel logic by electrically addressing the electronic states of a dopant atom. A single electron transistor decodes the physical multivalued output into the conventional binary output. A robust scalable circuit of two concatenated full adders is reported, where by utilizing charge and quantum degrees of freedom, the functionality of the transistor is pushed far beyond that of a simple switch.

cascading full adder | CMOS technology | energy and charge quantization

In digital logic circuits, binary information is encoded by monitoring the current, on vs. off, through a transistor that serves as a switch. This concept has been extremely effectively scaled over the last decades and led to the exceptionally dense and low cost integrated circuits that we use today. Decreasing the physical size of the component transistors has largely enabled the miniaturization. The reduction in the size of conventional transistors will shortly face the barrier that on the subnano length scale matter is discrete. The atomistic nature of matter leads to variability in device characteristics, which is the major problem in device downscaling. As we approach the physical limits of two-dimensional circuits essentially new paradigms are needed to sustain the rate of progress that our society has become used to. Here we utilize the discrete nature of matter at the atomic scale to offer a viable solution. Deterministic doping (1–3) emerges as a technique that overcomes variability problems (4). Furthermore, single atom doping allows for device functionality that exceeds that of a simple switch. This functionality of single-atom transistors, SATs, is robust due to the strong natural confinement of the Coulomb potential of the dopant. We connect the basic units, the SATs, with gain thereby allowing for a scalable circuit. It is because of the nature of SATs that our innovative Si device and experimental design can significantly accelerate the transfer of the new paradigm for device architecture from the laboratory to the R and D department.

Increasing integration and logical complexity and shrinking the size and the power requirements of computational networks are key desiderata of current information technology. There is therefore a world-wide intense research effort aiming at computing at the nano-scale, using both classical and quantum computing approaches (5–17). These advances are made possible by a complementary effort on building atomic devices and memory (3, 18–23).

Our work is based on the experimental work on SATs (24) and by general (25) and specific (26, 27) theoretical developments in electrical addressing of single nanodevices. Our SAT relies on distinguishing the occupancies of different quantum states of the dopant atom. Therefore we do not need to know the quantum phase that is conjugate to the quantum number.

An alternative approach to electrical addressing and one that allows for higher speeds of switching is to use optical signals as inputs. Optical addressing has been mostly applied to gas phase or solution ensembles (5, 7, 28, 29) and it is not well developed for addressing surface mounted circuits (30–32). The analysis of the operation of an experimental realization of a full adder in the gas phase using electronic spectroscopy (33) is also based on the physics of a multilevel system. Another multilevel logic scheme is based on different vibrational modes in a polyatomic molecule (34). The fundamental and crucial advance is that here we report on the response of a single atom and not of an ensemble as is the case for addressing in the gas phase or in solution.

There are two essential conceptual ingredients in our approach (35). *One* is the implementation of an entire logic circuit, rather than a switch, at the single nano-device level, that can be a molecule or a confined quantum system. We do so by taking advantage of the quantum mechanical inherently discrete energy structure of such nanosystems. This multi-physical-level structure enables the implementation of multivalued logic schemes. In other words, for us the need to design small scale devices is not a challenge but is an inherent characteristic of the solution. The *other* ingredient is concatenation: the communication of the output from one circuit as an input to the next circuit. This cascading, that as we show is accompanied by gain, allows the design of integrated circuits. A very early example is the experimental concatenation of two half adders to implement a full addition (36). Each half adder operates on the electronic levels of a chromophoric molecule. The addressing is by optical excitation from the ground to excited electronic states. Concatenation was achieved by resonant electronic energy transfer between two nonidentical chromophores. The pivotal point here is that the concatenation is not limited to the cascading of two devices. Because we have gain it can go on meaning that the design is fully scalable.

The functionality we report is equivalent to that of a 28 complementary-metal–oxide–semiconductor (CMOS) 1 bit full adder (37) and is implemented on a five transistor circuit, it is electrically addressed and read and the design is CMOS based. At the center of each logic unit is a single-dopant-atom transistor where the very few other nano transistors are needed to make it a realistic circuit, namely that it accepts and delivers to the next circuit binary signals as voltage (and not as current). Thereby the circuit exhibits gain.

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The Full Addition Implemented on a Single-Atom Transistor
A full adder is a logic circuit that accepts three binary inputs and forms their arithmetic sum. Two input variables, say A_i and B_i, are the 2 bit to be added in step i. There are four possible pairs of input values, A_iB_i 00, 01, 10, and 11. The third input, C_{i-1}, is the carry-in digit from a previous addition, step $i-1$. The essence of the function of the full adder is to perform the arithmetic sum of the three input variables. So the four possible values of the output are 0, 1, 2, and 3, the truth table for this operation is given in Table 1.

The Half-Adder. The half-adder operation, that is the summation with $C_{\text{in}} = 0$ is performed by the SAT. Our aim is to use the SAT to deliver a current that is the arithmetic sum of the two input digits. This sum can be 0 (input 0,0), 1 (input 0,1 or 1,0), or 2 (input 1,1). The essence of the physics is to tune the energy of the ground and of the first excited level of the dopant atom with the gate voltage such that no level or only one or both levels are resonant with the voltage gap between the source and drain electrodes, Fig. 1*B* (25). As is to be expected and as reviewed theoretically in *SI Text* and experimentally demonstrated in Fig. 1*B*, the current is essentially directly proportional to how many levels of the dopant atom are confined within the voltage window. We get a multilevel current corresponding to the arithmetic sum from the SAT, Fig. 1*A*, by mapping the inputs A and B onto the gate and bias voltages of the SAT. The gate electrode controls the energy levels of the dopant with respect to the electrochemical potential of the source and drain electrodes. Fig. 1*B* shows two clear current steps in the current, which are due to transport through the ground state and through the first electronic excited of the neutral dopant atom (24, 38). This stepwise behavior of the current is the physical basis for the multivalued processing of the addition of the two binary numbers A and B. These inherent plateaus in current allow us to robustly encode the logic inputs onto the gate and bias voltages as shown in Fig. 1*C*, something that is not possible in classical devices, e.g., Field Effect Transistor (FETs), because their transfer function is continuous.

The Full Adder. Without the need of concatenation we could have stopped here because the current through the SAT identified as I in Fig. 1 is the three valued variable that is the arithmetic sum (=the number of ones in the inputs) of A and B, see Table 1. Our aim however is to demonstrate a true balanced, concatenated device prototype and because the inputs are voltages we convert the output current to a voltage, identified as V_i in the circuit diagram in Fig. 1*D* by passing the current through a transistor that acts as a load resistance, R_L.

A full addition combines the multivalued current produced by the SAT with the current delivered from the FET representing the carry-in digit, see Fig. 2. The carry-in FET and the load resistor are combined in the Carry-In Buffer (CIB), which allows us to cascade the arithmetic sum of the previous operation with gain. We chose the threshold of the carry-in FET such that it is open in the case where the arithmetic sum of the previous operation is larger than 1. Because the carry-in FET and the SAT are placed in parallel, the total current through the load resistor, and hence the voltage V_i across it, corresponds to the arithmetic sum $A_i + B_i + C_{i-1}$. At this point we have a balanced full addition with experimental results shown in Fig. 3.

Decoding the Sum. The four-valued voltage, where experimental results are shown in Fig. 3, clearly allows a reading of the four possible results of a full addition. But to implement a device that is compatible with conventional circuits we add a decoder circuit, within a dotted frame and marked 3 in Fig. 2. Decoding is done by making use of the periodic Coulomb oscillations of a single electron transistor as function of gate voltage. The voltage V_i, corresponding to the arithmetic sum is applied to the gate of the SET (see Fig. S3 for more detail) resulting in a current through the SET that corresponds to the binary sum S in Table 1, see Fig. 3 *A* and *B*.

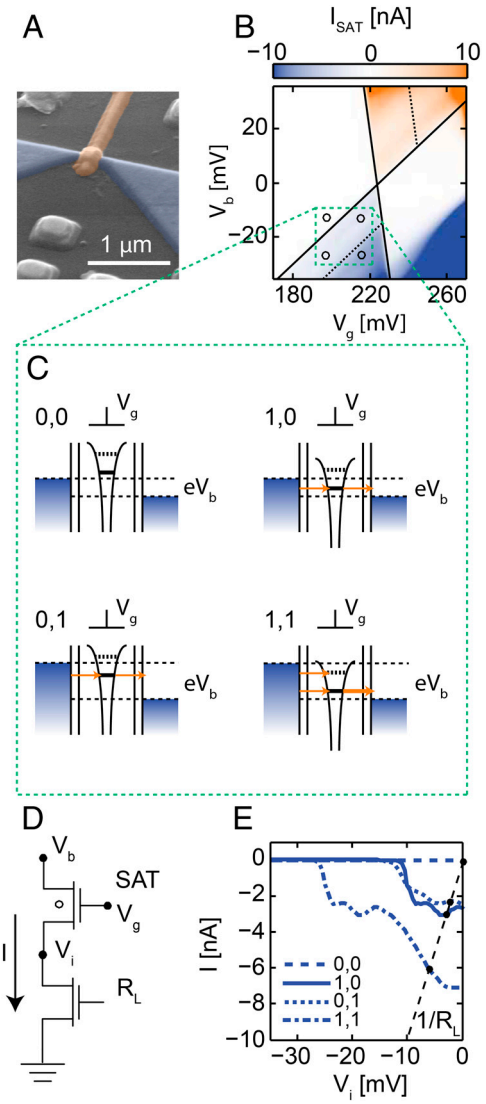

Fig. 1. (*A*). A scanning electron micrograph of a SAT. A SAT is a multigated field effect transistor commonly known as FinFET. (*B*). A measured stability diagram of the first electron in the SAT. The logic inputs (*A*) and (*B*), representing the two binary digits to be added, are mapped onto the gate and source-drain voltages. (*C*). Schematic energy diagram of the dopant energy levels with respect to the window between the source and the drain electrodes. The bias and the gate voltage each represent a binary variable, with a low (logic 0) and a high (logic 1) value such that when both V_b and V_g are low (a 0,0 input), there is no current flowing through the SAT because both values fall into the blocked region. When either V_b is high and V_g is low or vice versa (logic inputs 1,0 and 0,1 respectively), the current is finite. In that case the conduction occurs through the ground state (GS) only. The current is high when both input voltages are high (input 1,1) because then both the GS and the first excited state contribute to the transport. (*D*). The basic building block for our full adder consists of a SAT connected to a FET serving as load resistor R_L. (*E*). The current through the SAT and load resistor as a function of V_i for the inputs $V_g = 188$ mV, $V_b = -20$ mV (0,0), $V_g = 208$ mV, $V_b = -20$ mV (1,0), $V_g = 188$ mV, $V_b = -35$ mV (0,1), and $V_g = 208$ mV, $V_b = -35$ mV (1,1). The dots indicate for which V_i the current through the SAT and the FET are equal. V_i depends on FET resistance R_L that can be controlled by the FET gate voltage. The inherent plateaus in current as function gate and bias voltage allow for a robust encoding of inputs (*A*) and (*B*), in such a way that inputs 1,0 and 0,1 yield the same result, which is required for the half-addition.

Table 1. The truth table for a full addition, including the arithmetic sum (a.s.) and binary sum *S* and carry-out bit C_{out}

A	*B*	C_{in}	a.s.	C_{out}	*S*
0	0	0	0	0	0
0	1	0	1	0	1
1	0	0	1	0	1
1	1	0	2	1	0
0	0	1	1	0	1
0	1	1	2	1	0
1	0	1	2	1	0
1	1	1	3	1	1

Two Full Additions by Means of Concatenation

Of the four transistors that we require to produce a balanced scalable full adder, fully three are dictated by practical considerations such as gain, CIB_i, and the decoder circuit producing a binary rather than a multivalued output. This complete circuit is to be compared with the 28 transistors of the conventional design.

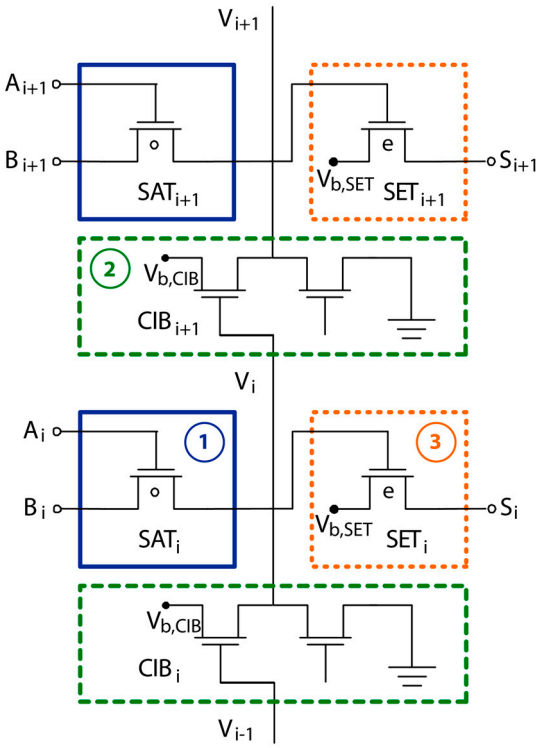

Fig. 2. Schematic circuit diagram of two concatenated full adders. The first adder unit, marked 1 and enclosed by a solid frame (blue online) adds binary inputs A_i and B_i using the occupancy of the orbital degrees of freedom of a single-atom in the SAT_i. The carry-in from the previous addition is added by the CIB CIB_i enclosed by a dashed frame (green online), this unit consists of two FETs that determine the gain of the system. In addition the CIB acts as a load for the SAT, resulting in a voltage V_i that corresponds to the arithmetic sum of inputs A_i, B_i, and C_{i-1}. The voltage V_i is fed into CIB_{i+1}, and thereby it is passed as a carry-in to the CIB of the next full adder circuit, (marked 2), upper part, $i+1$. The circuit enclosed by a dotted frame (orange on line), labeled 3, decodes from the voltage V_i the lump sum S_i using the periodicity of the response of a single electron transistor, SET_i. The output of the SET is a current that corresponds to the sum. This signal could be converted to a voltage by passing it through an additional load resistor. See *SI Text* for more details on the operation of the circuit. Each SAT is an industrial 32 nm node transistor. From the 32 nm half-pitch we can calculate that the area per transistor is 64×64 nm^2, therefore the footprint of a five transistor circuit is 0.02 μm^2. The essential advantage is however not in the size of the transistor, but in the fact that we use fewer of them, because of the increased functionality per device.

As we have demonstrated before, just the hybrid of one SAT and a FET can implement the essence of the operation of a full adder.

Only the ground and the lowest excited state of the dopant atom are used to implement the addition. Thereby the SAT performs a half adder. The carry-in is added through the current provided by the FET when the carry-in voltage is on. This design insures a very robust operation but including the FET transistor is not essential. The dopant atom has additional, resolvable, higher excited states (24). We have shown theoretically, both in general (25) and specifically (26) that one can electrically address a full adder. Furthermore, we have previously experimentally demonstrated a full adder operating on a single SAT (26). The use of a FET to bring in the carry voltage is to insure gain when the device is scaled. We need gain because we do not use an ensemble but concatenated single-atom devices. The measured output voltage resulting from a second full addition cascaded with the first one is showed in Fig. 2 *C* and *D*. The measurements prove that the experimental cascade is possible and efficient and that the circuit is scalable.

In summary, we demonstrated that using single-dopant-atom transistors it is possible to reduce the number of transistors in a logic circuit significantly. We built a full adder around a single SAT and then cascaded two such full adder circuits. Because the inputs and outputs are voltages, the device is scalable and can be part of an integrated circuit as in CMOS technology. The example chosen is that of the cascading of two full additions, where the carry-out of the present addition becomes the carry-in for the next one. An essential aspect of the logic design that reduces the number of transistors is to implement directly the logic operations at the hardware level and not to decompose them into circuits of switches. Using multivalued logic to take

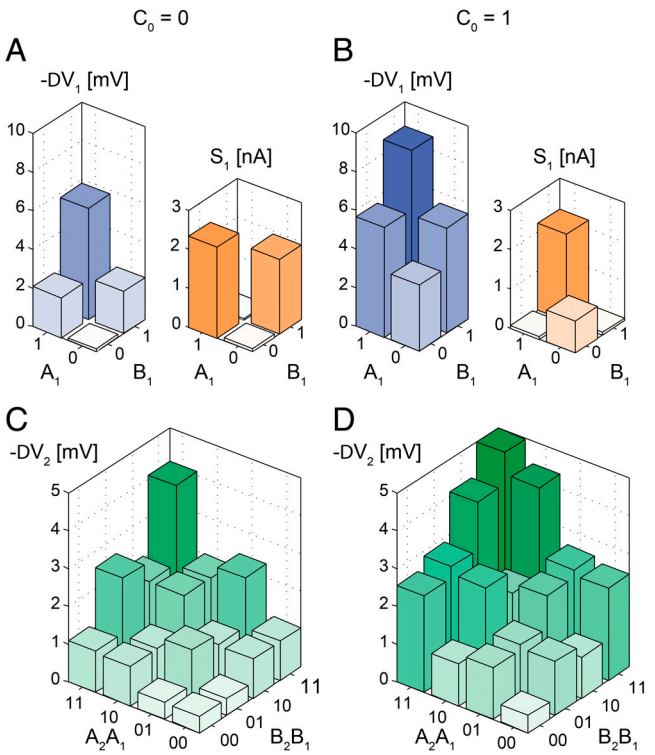

Fig. 3. Experimental results for the operation of a full adder (top, boxes *A* and *B*) and two concatenated full adders (bottom, boxes *C* and *D*). The top box shows the four values of voltage V_1 corresponding to the four-valued sum of the inputs A_1, B_1, and C_0 (see blue box in Fig. 2) and the current through the SET (see dashed orange box in Fig. 2), corresponding to the binary sum output with more details in the *SI Text*. The bottom box show the four values of voltage V_2 corresponding to the four-valued arithmetic sum of $A_2A_1 + B_2B_1 + C_0$. This output corresponds to V_{i+1} in Fig. 2.

advantage of the quantization of the energy levels of the dopant atom is the key ingredient that allows the reduction in the number of transistors. We also take advantage of charge quantization in the decoding of the sum out from the four-valued voltage output, thereby demonstrating a second type of concatenation, from a SAT adder to a SET decoder. Operating at the nano-scale and relying on energy, SAT, and charge, SET, quantization leads to a full adder circuit where the device functionality of the transistors goes far beyond that of a simple switch. Moreover, because the circuit is CMOS compatible, we can adapt the existing technology for the interface of the nano-scale with the macroscopic world.

Methods

The experimental demonstration is carried out on the levels of an arsenic atom (24) in a FinFET transistor (39). Typical energy spacings of the As atom dopant in the Si solid are of the order of few meV (1 meV = 11.6 K), which requires operating at liquid helium temperatures, because the level spacing needs to larger than the thermal broadening (40). Because of the random nature of dopant diffusion into the channel, we handpicked SATs suitable for our experiment. However, deterministic doping is rapidly emerging as technique that overcomes these kinds of device-to-device variability issues (1, 3). Moreover, efforts towards room-temperature quantum effects have been demonstrated in ultrascaled FinFET devices, where the level spacing due to confinement is comparable to the thermal energy at room temperature (41).

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